

Jinming Ren

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EDUCATION

University of Electronic Science and Technology of China (UESTC)	Sept 2022 — Present
University of Glasgow, Dual Degree Program	Sept 2022 — Present
<ul style="list-style-type: none">Major: Electrical & Communication Engineering BEng; GPA: 3.87/4.0, Ranking: 2/164 (Top 1.2%).Relevant Coursework: Signals and Systems, Stochastic Processes, Artificial Intelligence and Machine Learning, Information Theory, Electrodynamics, Digital Circuit Design, etc.Online Course: Abstract Algebra, Complex Analysis, Differential Geometry, Control Theory, etc.	

RESEARCH & PROJECTS

System-level Co-Design of RISCV Accelerators for TinyML at the Edge	Ongoing
<i>Research Assistant, Professor Yun Li, UESTC</i>	
<ul style="list-style-type: none">Designing, implementing and verifying hardware-accelerated depthwise-separable convolution (DSC) and attention kernels in ViT using C++ with RVV intrinsics that are adaptable and efficient for edge computing in Coral NPU framework open-sourced by Google and VeriSilicon.Exploring CUDA-like DSL to RVV ISA compiler for seamless deployment of TinyML models on RISCV-based NPUs.	
YOPO: You Only Pick Once – Light Object Tracking Algorithm	
	Sept 2025
<ul style="list-style-type: none">Developed a lightweight object tracking algorithm that requires only one initial selection, successfully mitigate the intense computation of DNN forward propagation on every frame.Utilized NCC-based matching, adaptive kernel updating, capable of tracking objects with gradual color and size changes.	
Control and Computer Vision for Autonomous Quadcopter System	Feb 2025 — Jun 2025
<ul style="list-style-type: none">Developed an automatic quadrotor aircraft for objection detection, route planning, and closed-loop flight control.Used ROS2 and OpenCV library to implement originally designed computer vision algorithms for real-time landing area detection.	
Design and Visualization of a Complete Single-cycle RV32I CPU Core	Jan 2025 — Mar 2025
<ul style="list-style-type: none">Designed and open-sourced an single-core, single-cycle RISCV 32-bit CPU from scratch in Verilog for RTL simulation and in Digital Software for working principle visualization.Built a complete datapath including PC, fetcher, decoder, register file, ALU, LRU-based L1 cache, etc., compatible with basic peripherals: GPIOs, IIC, UART, etc.Implemented a boot program in RISCV assembly, basic delay and gpio libraries in C. Compiled and simulated using RISCV GNU toolchain.	
CNN for Embedded Systems	Feb 2024 — May 2024
<ul style="list-style-type: none">Integrated a convolutional neural network (CNN) into STM32 MCU using C in MbedOS.Enabled smart fall detection, body temperature monitoring and real-time data visualization for patients.	

RELEVANT SKILLS

IT Skills	Latex, Quarto Markdown, Typst, Manim, Github.
Programming	C/C++, Python, RISCV Assembly, Verilog, Makefile, Bazel, Chisel, Matlab.
Language	Native Chinese, Fluent English.

AWARDS

Top Academic Scholarship of UESTC (Top 5%)	Dec 2023, Dec 2024
China National Scholarship (Top 3%)	Dec 2024
First Prize: 7th National College Art Exhibition and Performance	Sept 2024